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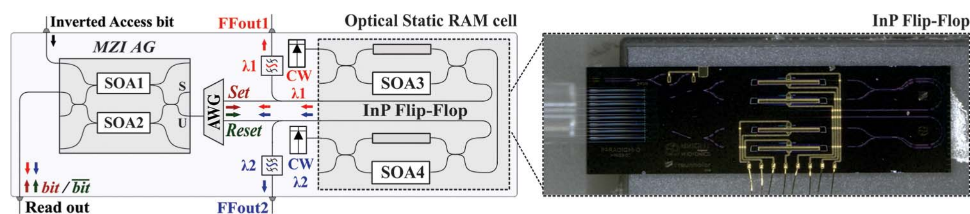

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WDM-Enabled Optical RAM at 5 Gb/s Using a Monolithic InP Flip-Flop Chip

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Abstract: We experimentally demonstrate an all-optical static random access memory (RAM) cell using a novel monolithic InP set–reset flip-flop (FF) chip and a single hybridly integrated semiconductor optical amplifier-Mach–Zehnder interferometer (SOA-MZI)-based access gate employing wavelength division multiplexing (WDM) data encoding. The FF device is a 6×2 mm^2 InP chip having a 97.8% reduced footprint compared with previous FF devices that were successfully employed in optical RAM setups. Successful and error-free RAM operation is demonstrated at 5 Gb/s for both READ and WRITE functionalities, having a power penalty of 4.6 dB for WRITE and 0.5 dB for READ operations. The theoretical potential of this memory architecture to allow RAM operation with memory speeds well beyond 40 GHz, in combination with continuously footprint-reducing techniques, could presumably lead to future high-speed all-optical RAM implementations that could potentially alleviate electronic memory bottlenecks and boost computer performance.

Index Terms: Mach–Zehnder interferometer (MZI), optical coupled switches, optical memory, optical RAM, semiconductor optical amplifier (SOA).

1. Introduction

With chip multiprocessor (CMP) architectures and resource disaggregation being the mainstream energy-efficient architectural scheme towards exaflop high-performance computing [1], computing is gradually turning into a network-dominated environment where processing relies on a large amount of core-to-core and core-to-memory transactions. This has brought interconnect technology right on the spot of the computing industry, with the substitution of electronic interconnects with optics [2] at deeper on-board and even on-chip hierarchy levels appearing as the dominant but still challenging technology solution [2]. This approach is also being promoted towards relaxing the limitations arising by the Memory Wall problem [4] that refers to the discrepancy observed on the rate at which the processing and the electronic memory speeds increase. Replacing the slow electrical buses between processors and memory units with optical technologies [5], [6] can scale-up the transaction bandwidth addressing the von Neumann bottleneck [7] through reduced latency values in memory access.

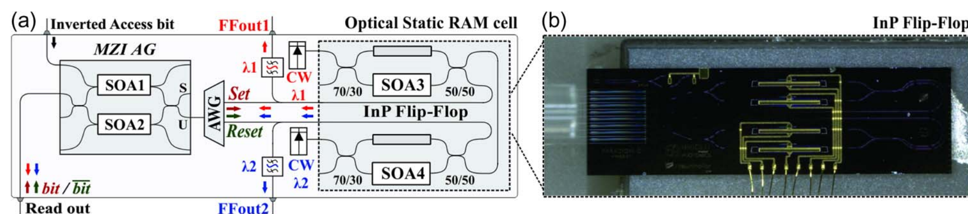

Fig. 1. (a) Experimental layout of optical static RAM cell incorporating the SOA-MZI AG and the InP FF. (b) Packaged monolithic InP FF chip (AWG) forming the Set and Reset signals that are subsequently guided to the FF.

Following this roadmap, the next step beyond the optically interconnected memories for matching processing with memory fetching speeds should target the seamless interaction between the optical link and memory chips, favoring the use of ultra-fast all-optical memory modules that can store and retrieve information directly in the optical domain. This pathway has been already indicated recently at system-scale revealing important speed-up benefits when using optical cache memory layouts in CMPs [8], [9]. To this extent, several state-of-the-art photonic memories have been demonstrated so far following different technological approaches in order to reflect into the needs of speed, footprint, scalability and power consumption. Until now, several latching mechanisms have been investigated, including wavelength bistability in photonic crystals (PhC) [10], direction bistability in ring lasers [11], coupled ring-lasers in a master-slave configuration [12], polarization bistability in vertical cavity surface emitting lasers [13] and lately phase bistability in phase change materials (PCM) [14] that has been proposed towards non-volatile photonic memory solutions. However, most of them have been mainly limited to elementary latching demonstrations with practical random access memory (RAM) implementations having been shown only by means of coupled optical switch layouts [15]–[17]. Besides revealing the enhanced maturity level of coupled switch memory configurations, these demonstrations have also triggered a series of novel architectural schemes with respect to RAM Access Gate (AG) and peripheral circuitry [18]–[21] introducing wavelength division multiplexing (WDM) in the caching landscape. However, optical RAM demonstrations have so far relied on rather bulky fiber-based or hybridly integrated flip-flop arrangement with the WDM-enabled shared AG concept having been shown either in standalone AG experiments [18] or with Mb/s-scale fiber-based flip flops [22], still lacking an experimental confirmation in Gb/s-scale integrated memory setups.

In this paper, we present an optical static RAM cell at 5 Gb/s using a monolithically integrated InP FF and a single semiconductor optical amplifier-Mach–Zehnder Interferometer (SOA-MZI) AG that exploits wavelength diversity at both stored and retrieved data signals. The InP FF chip comprises two coupled SOA-MZI switches and has a total footprint of 6×2 mm^2, suggesting a 97.8% footprint reduction compared to the hybrid FF used in the first optical RAM cell demonstration [15], where a 45×12 mm^2 hybrid FF was incorporated [23]. The waveguide used for coupling the two switches had a length of 5 mm being 5× lower than the respective length of the hybridly integrated FF and raising expectations for higher RAM operational speeds, limited only by the SOA response time [24], [25]. Successful error-free operation for both READ and WRITE functionalities at 5 Gb/s has been obtained with power penalty values of 0.5 dB and 4.6 dB, respectively.

The rest of the paper is organized as follows: Section 2 describes the RAM cell layout, the operation principle and the experimental setup used for the RAM cell evaluation; the WRITE operation and the READ operation respectively. Section 3 presents the experimental evaluation of the two aforementioned operation modes of the RAM cell.

2. Device and Experimental Setup

The optical static RAM cell layout is shown in Fig. 1(a) and comprises a hybridly integrated SOA-MZI used as the single AG and a monolithic InP chip that incorporates the all-optical FF [26].

During WRITE operation, the complementary data bit and $\overline{\textbf{bit}}$ signals are encoded on different wavelengths and enter the AG through a common input port. The Inverted Access signal gets injected through the respective Inverted Access bit port acting as the control signal of the SOA-MZI AG and allowing or blocking the bit and $\overline{\textbf{bit}}$ signals from exiting the AG switch. When the Inverted Access bit has a logical “1” value, the AG operates in its switching state forcing the bit and $\overline{\textbf{bit}}$ signals to emerge at the S-port of the AG without allowing them to appear at the U-port and to continue towards the FF. In the absence of an Inverted Access bit, the bit and $\overline{\textbf{bit}}$ signals exit the AG through its U-port and are then demultiplexed in an Arrayed Waveguide Grating.

The FF follows a typical master-slave coupled switch configuration [22] consisting of two SOA-MZI switches that have two of their output ports coupled together via a waveguide section. Every SOA-MZI switch has a single SOA (SOA3 or SOA4) at one of its branches and an electrically controlled phase section at its second branch to allow for optimally balancing the interferometer. Two CWs at $\lambda 1$ and $\lambda 2$ are entering the two switches as input signals serving as the corresponding DC power supply signals used in conventional electronic latching elements. The Set and Reset signals are counter propagating with respect to the $\lambda 1$ and $\lambda 2$ CW signals, respectively, deciding upon the memory state. The FF content during WRITE functionality can be monitored at the FFout1 and FFout2 output ports of the RAM cell after having been filtered in respective optical bandpass filters (OBPFs) centered at $\lambda 1$ and $\lambda 2$.

The same RAM cell layout is used also for READ operation, where no bit and $\overline{\textbf{bit}}$ signals are entering the cell. In that case, the FF output signals carried by $\lambda 1$ and $\lambda 2$ wavelengths are entering the AWG ports and are then multiplexed into a common stream that gets inserted into the AG through its U-port. The Inverted Access bit signal serves again as the AG control signal dictating whether the memory content emerging at the AG U-port will be allowed to appear at the Readout port of the AG. In the case of a high value for the inverted access bit, the memory content gets blocked, while a low logical value used as the inverted access bit allows the memory content to transit the AG yielding successful READ operation.

The FF has been fabricated as a monolithically integrated InP chip within a multi-project wafer (MPW) run of the EU-funded project PARADIGM and is depicted in Fig. 1(b). The chip was designed and fabricated using library-based non-optimized components in a monolithic integration procedure, suggesting the potential to fabricate in the same integration platform more complex and complete photonic memories that encompass different types of subsystems. It has a footprint of only 6×2 mm^2 and the two SOA-MZI switches that form the FF were coupled together via a 5 mm long InP waveguide. SOA3 and SOA4 devices had each one 1 mm length. The couplers at the input stages of the MZIs where the CW DC signals are launched had a cross/through splitting ratio of 70/30 while the output coupling stages of the intra-FF coupling stage between the two MZIs, where also the Set/Reset signals are launched featured a 50/50 coupling ratio. The SOAs of the FF had an output saturation power of 5 dBm, gain recovery time of 77 ps and polarization gain dependence of 12 dB while operating at 280 mA regime. The FF device was fiber pigtailed using a fiber array of 127 μm pitch attached to edge spot size converters, while the overall butt-coupling losses including the small signal gain of the SOA with respect to the input/output power are 2 dB [26]. The SOA-MZI used as the AG was fabricated as a hybridly integrated silica-on-silicon device incorporating two 1.6 mm-long SOAs (SOA1 and SOA2) exhibiting 12.5 dBm output saturation power and gain recovery time of 70 ps while both operating at 250 mA.

In order to prove the RAM cell operation for WRITE and READ memory functionality, two different experimental setups were formed. In Fig. 2, the respective setup for evaluating the WRITE operation is depicted. A signal generator (SG) is used to drive the programmable pattern generator (PPG) at 5 GHz. The PPG is driving the two Ti:$LiNbO_3$ modulators complementary in order to produce the 5 Gb/s 2^7-1 PRBS NRZ signals. The first modulator is responsible for producing the Inverted Access bit signal at 1554.8 nm and the bit signal at 1558.7 nm while the second for the $\overline{\textbf{bit}}$ signal at 1557.9 nm. The three signals are reaching, through a coupler, two different branches each one comprising an erbium-doped fiber amplifier (EDFA). The first

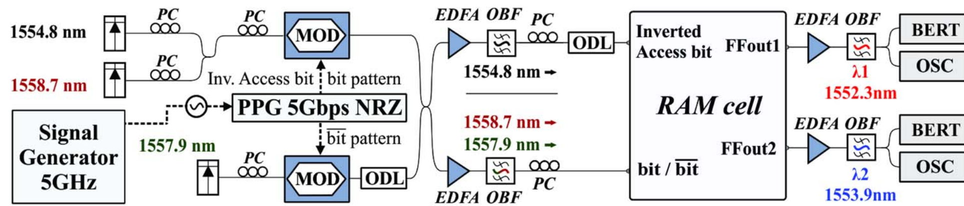

Fig. 2. Experimental setup for the evaluation of the WRITE operation.

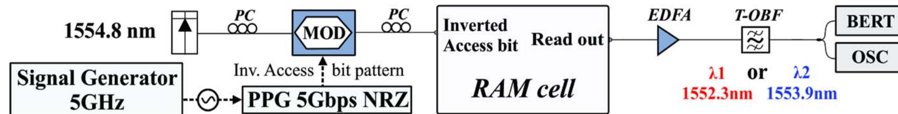

Fig. 3. Experimental setup for the evaluation of the READ operation.

branch incorporates a 0.6 nm 3 dB-bandwidth OBF centered at 1554.8 nm to properly filter the inverted access bit signal before reaching the respective input port of the RAM cell. The second branch incorporates a 1 nm 3 dB-bandwidth OBF centered at 1558.3 nm and is responsible for filtering the two complementary bit/$\overline{\textbf{bit}}$ signals before reaching the RAM cell bit/$\overline{\textbf{bit}}$ ports. The AWG that is used to form the experimental setup of the RAM cell has a 0.65 nm 3-dB channel bandwidth. The RAM cell memory content signals emerging at the FFout1 and FFout2 output ports were then amplified in respective EDFAs and filtered in 0.6 nm 3 dB-bandwidth OBPFs centered at $\lambda 1 = 1552.3$ nm and $\lambda 2 = 1553.9$ nm, respectively, prior being recorded by a digital sampling oscilloscope (OSC) and used for bit error rate evaluation purposes in a bit error rate tester (BERT). Polarization controllers (PC) were used throughout the whole experimental setup to maintain proper signal polarization at several stages of the setup. variable optical attenuators (VOA) were also used to properly adjust and the power levels of the optical signals, while optical delay lines (ODLs) were employed to ensure signal decorrelation and bit-level synchronization.

Fig. 3 illustrates the experimental setup used for evaluating the READ functionality. A Signal Generator (SG) is used again to drive the PPG at 5 GHz. The PPG is driving the Ti:$LiNbO_3$ modulator in order to produce the 5 Gb/s 2^7-1 PRBS NRZ pattern used as the inverted access bit control signal to enter the RAM cell. To evaluate the READ operation, the FF is each time set to one of its logic memory states by properly adjusting the external CW signals power-levels, meaning that either only $\lambda 1$ or $\lambda 2$ is the dominant wavelength in the FF providing high FF output power level either at the FFout1 or at the FFout2 port, respectively. A monitor branch is connected at the Readout port of the RAM cell comprising an EDFA as a preamplifier and a 0.6 nm 3 dB-bandwidth tunable OBPF (T-OBPF) that can be tuned either at $\lambda 1$ or at $\lambda 2$ in order to evaluate each time the Read-out signal at the corresponding wavelength. PCs and VOAs are once again used for polarization and power level management purposes.

3. Experimental Results and Evaluation

Fig. 4 depicts the experimental results obtained for both WRITE and READ operation of the RAM cell experiment at 5 Gb/s. Fig. 4(a)–(g) depict the time traces and their respective eye diagrams of the signals that verify the WRITE mode operation. Fig. 4(a) shows the inverted access bit signal that is introduced as the control signal at the SOA-MZI AG, while Fig. 4(b) and (c) show the complementary bit/$\overline{\text{bit}}$ sequences that represent the data bit stream to be written in the RAM cell. The inverted ON-OFF gating upon bit/$\overline{\text{bit}}$ signals is logically imprinted on the Set and Reset signals, as shown in Fig. 4(d) and (e). The jitter observed at some of the pulses in the eye diagrams of the set/reset signals is observed after a pulse of inverted access signal becomes extinct, and stems from the recovery time of the SOA [18]. Fig. 4(f) and (g) illustrate the FF output

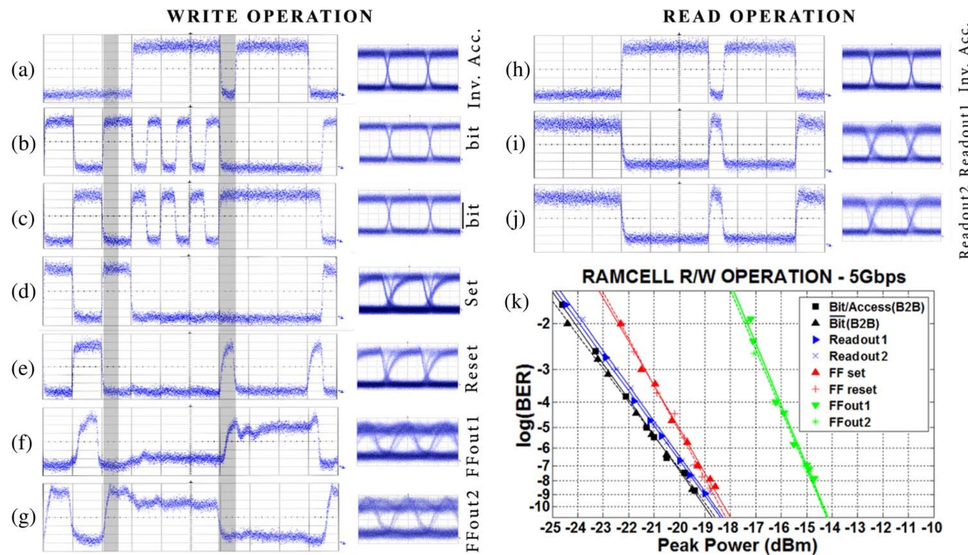

Fig. 4. (a)–(g) Time traces (400 ps/div) and eye diagrams (50 ps/div) for WRITE operation. (h)–(j) Time traces (400 ps/div) and eye diagrams (50 ps/div) for READ operation. (k) BER measurements for READ/WRITE operation at 5 Gb/s.

results as recorded at FFout1 and FFout2 monitoring ports of the RAM cell at $\lambda 1 = 1552.3$ nm and $\lambda 2 = 1553.9$ nm. Whenever a "0" inverted access bit enters the AG, the Set and Reset signals are identical to the incoming bit/$\overline{\text{bit}}$ streams content. The memory content in this case follows the pattern of the Set and Reset signaling. Whenever a "1" inverted access bit enters the AG turning the AG to its "Off" state, the Set and Reset signals are blocked and the RAM cell retains the last induced memory state until a new Set of Reset pulse arrives. The grey-highlighted areas in Fig. 4(a)–(g) highlight cases where data are transmitted through the AG and the Set and Reset signal values are following the respective values of the bit and $\overline{\text{bit}}$ signals. The left highlighted area depicts a Set pulse-induced state change of the FF, while the right highlighted area a Reset pulse-induced state change of the FF. Open eye diagrams are obtained for all signals, revealing an extinction ratio of 9.2 dB for the Inverted Access bit, the bit and the $\overline{\text{bit}}$ signals, 9 dB for the Set and Reset signals and 6 dB for the FFout1 and FFout2 signals.

Fig. 4(h)–(j) correspond to the results of the READ operation. Fig. 4(h) depicts the Inverted Access bit signal that is applied on the RAM cell, while Fig. 4(i) and (j) show the time traces and eye diagrams of the stored bit signals emerging at the Readout port of the RAM cell when either $\lambda 1$ or $\lambda 2$ dominate the FF, respectively. Both cases reveal successful READ functionality with negative logic operation [18], i.e., access of the stored FF-content to the READ output is granted when the Inverted access signal features a logical "0," resulting in complementary time-traces for the Readout signals. Open eye diagrams for the READ operation were obtained, featuring an extinction ratio of 9.2 dB for the Inverted Access bit signal and 9 dB for both of the FF states.

Although the use of a discrete AG fiber-interconnected to a monolithic integrated FF-device introduces some latency, it allows overcoming the main-speed determining factor of the large intra-FF coupling distance [24] and facilitates evaluating the READ and WRITE RAM operations independently without any speed limitation, when unidirectional data-communication is employed. In case of a fully integrated RAM cell, shorter latency between the AG and the FF would enable studying READ and WRITE functionalities simultaneously, while faster operational speed could only be further improved by incorporating high-speed SOAs in the current architecture [24].

The BER diagrams of the RAM cell evaluation both in WRITE and READ operations are illustrated in Fig. 4(k). The BER diagrams show a 10^{-9} error-free operation with a power penalty of 4.6 dB for the data written in the RAM cell, while the Set and reset signals had a power penalty

of 0.6 dB at the SOA-MZI AG output. In the case of READ mode operation, error-free operation was obtained again with a power penalty of only 0.5 dB at an error-rate of 10^{-9}.

For the experimental evaluation of the RAM cell functionality during WRITE operation, the power levels of the inverted access bit, the bit and the $\overline{\textbf{bit}}$ signals entering the AG were measured to be 0 dBm, −4 dBm and −4 dBm, respectively. The average powers of the $\lambda 1$–$\lambda 2$ CWs entering the FF were measured to be 7 dBm and 13 dBm, respectively, while the peak power of the Set-Reset signals was 16 dBm and 12 dBm, respectively. The AG SOAs (SOA1 and SOA2) were electrically driven both at 250 mA, while the SOAs of the FF (SOA3 and SOA4) at 269 mA and 290 mA, respectively. In the experimental evaluation of READ mode operation, the measured power level of the inverted access bit entering the AG was again 0 dBm. The measured power of the two signals at $\lambda 1$ and $\lambda 2$ that emerge at the output of the FF was −4 dBm per wavelength before entering the AG. During READ operation, the SOAs of the AG were both electrically driven at a DC current of 250 mA, while in this operation, the two FF SOAs were both driven at 270 mA, compared to the 122 mA and 76 mA of the previously hybridly integrated FF.

4. Conclusion

We have presented an all-optical static RAM cell that consists of a monolithically integrated InP Set/Reset FF chip and a hybridly integrated SOA-MZI AG. The FF chip encompasses two coupled optical switches and exhibits 97.8% lower footprint with respect to previous optical FF devices employed in successful RAM cell implementations. Successful RAM cell operation at 5 Gb/s has been achieved using WDM-encoded data signals that share a common AG with power penalties of 0.5 dB and 4.6 dB for READ and WRITES functionality, respectively. Taking into account the recently demonstrated 10 Gb/s storage capabilities of the InP FF chip [25] and the 5 mm long coupling section between the intra-FF switches, which corresponds to a theoretically expected speed value of 40 GHz [22], this RAM cell layout raises expectations for operating at speeds beyond 10 Gb/s while requiring only three optical gates.

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